



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/557,520	01/30/2007	Minoru Ishikawa	1232-5791	8818
27123 7590 04/04/2008 MORGAN & FINNEGAN, L.L.P. 3 WORLD FINANCIAL CENTER NEW YORK, NY 10281-2101				
EXAMINER MOORAD, WASEEM				
ART UNIT		PAPER NUMBER		
2629				
NOTIFICATION DATE		DELIVERY MODE		
04/04/2008		ELECTRONIC		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOPatentCommunications@Morganfinnegan.com
Shopkins@Morganfinnegan.com
jmedina@Morganfinnegan.com

Office Action Summary

Application No.

10/557,520

Applicant(s)

ISHIKAWA ET AL.

Examiner

WASEEM MOORAD

Art Unit

2629

Period for Reply -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 November 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-85/86)
- Paper No(s)/Mail Date 11/14/05.
- 4) ☐ Interview Summary (PTO-413)
- Paper No(s)/Mail Date _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Sudo et al. (US 5,693,913).

Regarding Claim 1, Sudo et al. a coordinate input apparatus, comprising:
a plurality of X interconnecting lines and a
plurality of Y interconnecting lines disposed to intersect with each other in a matrix
fashion (column 2, lines 61-67);

a closed-loop forming circuit for being electrically connected with the X
interconnecting lines or the Y interconnecting lines so as to switchably connect a
predetermined number of the X interconnecting lines or a predetermined number of the
Y interconnecting lines to form a closed loop (Figure 7, where elements 511ab and
512ab form a closed loop circuit between a predetermined number of Y interconnecting
lines); and

a detection circuit for detecting a signal outputted from the closed loop in
response to a position indicator for indicating a position in a coordinate input area where
the X interconnecting lines and the Y interconnecting lines are disposed in the matrix

Art Unit: 2629

fashion (Figure 7, columns 21, lines 52-64, where the control circuit detects a signal outputted from the closed loop in response to the coordinate indicator's actions);

wherein the closed loop is a multiple closed loop (Figure 7, where elements 511 and 512 are a multiple closed loop).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sudo et al. (US 5,693,913) in view of Oda (5,646,377).

Regarding Claim 2, it is analyzed with respect to the analysis of Claim 1. Sudo et al. does not teach wherein the closed loop includes a switch circuit for selecting first to four X interconnecting lines from the plurality of X interconnecting lines so that: a first terminal of the first X interconnecting line is connected with a first terminal of the second X interconnecting line, a first terminal of the third X interconnecting line is connected with a first output terminal, a second terminal of the third X interconnecting line is connected with a second terminal of the first X interconnecting line, a first terminal of the fourth X interconnecting line is connected with a second output terminal, and a second

terminal of the fourth X interconnecting line is connected with a second terminal of the second X interconnecting line.

Oda teaches wherein the closed loop includes a switch circuit for selecting first to four interconnecting lines from the plurality of interconnecting lines so that: a first terminal of the first interconnecting line is connected with a first terminal of the second interconnecting line, a first terminal of the third interconnecting line is connected with a first output terminal, a second terminal of the third interconnecting line is connected with a second terminal of the first interconnecting line, a first terminal of the fourth interconnecting line is connected with a second output terminal, and a second terminal of the fourth interconnecting line is connected with a second terminal of the second interconnecting line (Figure 14c, where a double closed-loop circuit comprises a switch circuit from selecting a plurality of interconnecting lines and connects them accordingly. The first line is the 4th terminal, the second line is the 1st terminal, the third line is the 2nd terminal, and the fourth line is the 3rd terminal).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Sudo et al. with the teachings of Oda by having the plurality of X interconnecting lines connected in this manner so that this double loop configuration can provide improvement in absolute sensitivity and further the effect to cancel the errors owing to the position on the loop coil to some extent (column 23, lines 32-35)

Regarding Claim 3, it is analyzed with respect to the analysis of Claim 2. Sudo et al. does not teach wherein the closed loop includes a switch circuit for selecting first to four Y interconnecting lines from the plurality of Y interconnecting lines so that: a first terminal of the first Y interconnecting line is connected with a first terminal of the second Y interconnecting line, a first terminal of the third Y interconnecting line is connected with a first output terminal, a second terminal of the third Y interconnecting line is connected with a second terminal of the first Y interconnecting line, a first terminal of the fourth Y interconnecting line is connected with a second output terminal, and a second terminal of the fourth Y interconnecting line is connected with a second terminal of the second Y interconnecting line.

Oda teaches wherein the closed loop includes a switch circuit for selecting first to four interconnecting lines from the plurality of interconnecting lines so that: a first terminal of the first interconnecting line is connected with a first terminal of the second interconnecting line, a first terminal of the third interconnecting line is connected with a first output terminal, a second terminal of the third interconnecting line is connected with a second terminal of the first interconnecting line, a first terminal of the fourth interconnecting line is connected with a second output terminal, and a second terminal of the fourth interconnecting line is connected with a second terminal of the second interconnecting line (Figure 14c, where a double closed-loop circuit comprises a switch circuit from selecting a plurality of interconnecting lines and connects them accordingly. The first line is the 4th terminal, the second line is the 1st terminal, the third line is the 2nd terminal, and the fourth line is the 3rd terminal).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Sudo et al. with the teachings of Oda by having the plurality of Y interconnecting lines connected in this manner so that this double loop configuration can provide improvement in absolute sensitivity and further the effect to cancel the errors owing to the position on the loop coil to some extent (column 23, lines 32-35)

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sudo et al. (US 5,693,913) in view of Morita (US 5,128,499)

Regarding Claim 4, it is analyzed with respect to the analysis of Claim 1. Sudo et al. is silent regarding wherein the closed loop is sequentially formed at a constant pitch on the matrix of the X and Y interconnecting lines with a lapse of time.

Morita teaches wherein the closed loop is sequentially formed at a constant pitch on the matrix of the X and Y interconnecting lines with a lapse of time (Figure 1, column 3, lines 65-68; where the closed loop has a constant pitch, element Ps)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Sudo et al. with the teachings of Morita by having a closed loop formed at a constant pitch so to have equal conductivity between each of the sense lines on the X-Y matrix.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sudo et al. (US 5,693,913) in view of Watanbe et al. (US 5,567,920).

Regarding Claim 5, it is analyzed with respect to the analysis of Claim 1. Sudo et al. is silent regarding wherein on the matrix of the X and Y interconnecting lines, a closed loop formed timewise previously and a subsequent closed loop formed after the closed loop are selected to have an embedded structure.

Watanbe et al. teaches wherein on the matrix of the X and Y interconnecting lines, a closed loop formed timewise previously and a subsequent closed loop formed after the closed loop are selected to have an embedded structure (Figure 18, column 20, lines 22-32; where an embedded structure is formed with the closed loop and the subsequent closed loop)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Sudo et al. with the teachings of Watanbe et al. by having a closed loop and a subsequent closed loop to have an embedded structure so that electromagnetic coupling is cancelled (column 20, lines 28-32).

7. Claims 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sudo et al. (US 5,693,913) in view of Yoshida et al. (US 5,798,756).

Regarding Claim 6, it is analyzed with respect to the analysis of Claim 1. Sudo et al. is silent regarding wherein the coordinate input area is formed in a display panel

Yoshida et al. teaches the coordinate input area is formed in a display panel (column 7, lines 16-30; where the panel is an LCD panel)

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Sudo et al. with the teachings of Yoshida et al. by having the coordinate input area formed in a display panel in order to determine the coordinates of a display panel (column 7, lines 32-36).

Regarding Claim 7, it is analyzed with respect to the analysis of Claim 6. Yoshida et al. further teaches a circuit for switching a display drive mode using the matrix of the X and Y interconnecting lines and a coordinate detection drive mode using the matrix of the X and Y interconnecting lines (Figure 1, element 108; column 18, lines 19-25; where the changeover control circuit switches between the display driving circuit and the coordinate detection circuit).

8. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sudo et al. (US 5,693,913) in view of Yoshida et al. (US 5,798,756) and further in view of Kawai (US 2003/0086149)

Regarding Claim 8, it is analyzed with respect to Claim 6. Sudo et al., in view of Yoshida et al., does not teach the display panel having a memory characteristic.

Kawai teaches an electrophoretic display having a memory characteristic (page 1, section 0003).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Sudo et al., in view of Yoshida et al. with the teachings of Kawai by having a display panel having a memory characteristic so to have the ability to hold a display image (page 1, section 0003)

Regarding Claim 9, it is analyzed with respect to the analysis of Claim 8. Kawai further teaches the display panel being an electrophoretic display panel (page 1, section 0003).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WASEEM MOORAD whose telephone number is (571)270-3436. The examiner can normally be reached on M-F 730am-4pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2629

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Waseem Moorad/
Examiner, Art Unit 2629
/W. M./
Examiner, Art Unit 2629
03/25/08

/Amr Awad/
Supervisory Patent Examiner, Art Unit 2629